

**PSEUDO FAIL BIT MAP GENERATION FOR RAMS DURING COMPONENT TEST
AND BURN-IN IN A MANUFACTURING ENVIRONMENT**

Abstract of the Invention

5 According to an embodiment of the present invention, a method is provided for
determining a fail string for a device. The method includes determining a test pattern for
a portion of an address space wherein the test pattern includes at least one address in
the address space and the portion of the address space includes at least one x address
and at least one y addresses. The method executes a test a plurality of times for each
10 test pattern, wherein every combination of the test pattern is tested, wherein the
combinations include each address held at a first potential for at least a first test and a
second potential for at least a second test. The method includes determining a fail
string for the device including pass/fail results for the test pattern, and combining the
pass/fail results in the fail string.